DYNAMIC PHASE ALIGNMENT AND
CLOCK RECOVERY CIRCUITRY

[0061] A dynamic phase alignment circuit is provided that aligns data signals to a phase of a forwarded clock at each channel in a multi-channel communications protocol. A forwarded clock is sent to a phase locked loop (PLL) circuit that generates multiple clock phases of the forwarded clock. The dynamic phase alignment circuit selects the optimal clock phase with which to align an input data signal for transmission to the corresponding channel. The dynamic phase alignment circuit can also be used for clock recovery.